Roger Hsiao

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Education

University of California–Berkeley **2021 – Present**

Ph.D. in Electrical Engineering and Computer Science

- **Relevant Courses:** Deep Reinforcement Learning (CS 285), Applications of Parallel Computers (CS 267), Design Project: 16nm SoC for IoT (EE 290), Optimization Models in Engineering (EECS 227AT)

University of Michigan–Ann Arbor **2017 – 2021**

B.S. in Computer Engineering, summa cum laude

- **Relevant Courses:** Very-Large-Scale Integrated Design I (EECS 427), Very-Large-Scale Integrated Design II (EECS 627), Computer Architecture (EECS 470), Introduction to Operating System (EECS 482), Machine Learning (EECS 545)

Academic Research Experience

Second-Order Optimization of 3D Gaussian Splatting **August 2025 – Present**

Specialized Computing Ecosystems Lab *Berkeley, California*

- Developed templated library to compute Jacobian-vector products for any custom CUDA kernel through automatic differentiation
- Enabled large-scale Gauss-Newton's method for 3D Gaussian Splatting scene training

Algorithm-Hardware Co-Design for Resource-Aware SLAM **November 2023 – July 2024**

Specialized Computing Ecosystems Lab *Berkeley, California*

- Developed **SuperNoVA**, a full-stack algorithm-hardware co-design framework enabling real-time SLAM for edge devices
- Designed a resource-aware, incremental optimization algorithm that dynamically trades off accuracy for latency

Heterogeneous Robotics SoC Tapeout **October 2023 – August 2024**

Specialized Computing Ecosystems Lab *Berkeley, California*

- Designed and taped out **MAVERIC**, a custom 16nm heterogeneous System-on-Chip integrating 4 CPU cores and 13 INT8/FP32 accelerators
- Implemented memory-efficient algorithm to execute end-to-end perception and SLAM workloads on-chip

Backend Optimization for SLAM **January 2022 – Present**

Specialized Computing Ecosystems Lab *Berkeley, California*

- Implemented a fast, parallel Schur complement algorithm exploiting structured sparsity in large-scale SLAM problems
- Profiled Kimera-VIO with a GTSAM backend to identify and analyze computational bottlenecks
- Optimized GTSAM linear algebra kernels for improved performance and scalability
- Proposed a unified linear interface for SLAM backends to enable flexible hardware–software co-design

M3 Monarch Migration Study **January 2018 – June 2021**

Blaauw Lab *Ann Arbor, Michigan*

- Programmed the Michigan Micro Mote (M^3) system to collect environmental data mounted on monarch butterflies during fall migration
- Designed on-chip, real-time data processing and compression to store three months worth of data in 10kB of storage space

Publications

1 **Hsiao, R.**; Fang, Y.; Huang, X.; Li, R.; Rabeti, H.; Gojcic, Z.; Lavaei, J.; Demmel, J.; Shao, Y. S. 3DGS^2-TR: Scalable Second-Order Trust-Region Method for 3D Gaussian Splatting. ICML 2026.

2 Kim, S.; **Hsiao, R.**; Nikolic, B.; Demmel, J.; Shao, Y. S. SuperNoVA: Algorithm–Hardware Co-Design for Resource-Aware SLAM. *In Proceedings of the 30th ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Volume 1*; ACM: March 2025; pp 1035–1051.

3 Kim, S.; Zhao, J.; **Hsiao, R.**; Chi, Y.; Iyer, V.; Jain, V.; Nikolić, B.; Shao, Y. S. MAVERIC: A 16nm 72 FPS, 10 mJ/Frame Heterogeneous Robotics SoC with 4 Cores and 13 INT8/FP32 Accelerators. *In 2025 Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*; IEEE: 2025; pp 1–3.

4 Lee, I.; **Hsiao, R.**; Carichner, G.; Hsu, C.-W.; Yang, M.; Shoouri, S.; Ernst, K.; Carichner, T.; Li, Y.; Lim, J.; Julick, C. R.; Moon, E.; Sun, Y.; Phillips, J.; Montooth, K. L.; Green Ii, D. A.; Kim, H.-S.; Blaauw, D. Tracking the Migration of the Monarch Butterflies with the World's Smallest Computer. *GetMobile: Mobile Computing and Communications*, 2022, 26 (1), 25–29.

5 Lee, I.; **Hsiao, R.**; Carichner, G.; Hsu, C.-W.; Yang, M.; Shoouri, S.; Ernst, K.; Carichner, T.; Li, Y.; Lim, J.; Julick, C. R.; Moon, E.; Sun, Y.; Phillips, J.; Montooth, K. L.; Green, D. A.; Kim, H.-S.; Blaauw, D. "mSAIL: Milligram-Scale Multi-Modal Sensor Platform for Monarch Butterfly Migration Tracking." *In proceedings of the 27th Annual International Conference on Mobile Computing and Networking*; ACM: New Orleans Louisiana, 2021; pp 517–530. **Best Paper Award**

6 Yang, M.; **Hsiao, R.**; Carichner, G.; Ernst, K.; Lim, J.; Green, D. A.; Lee, I.; Blaauw, D.; Kim, H.-S. Migrating Monarch Butterfly Localization Using Multi-Modal Sensor Fusion Neural Networks. *In 2020 28th European Signal Processing Conference (EUSIPCO)*; IEEE: Amsterdam, Netherlands, 2021; pp 1792–1796.

Industry Experience

Fast-VGGT—Visual-Geometry Transformer for Real-Time 3D Perception **Summer 2025**
NVIDIA Robotics Software Intern *Santa Clara, CA*

- Implemented KV-cache for visual geometry grounded transformer model for robust, real-time localization and 3D reconstruction
- Discovered and profiled causal scale drift, a distribution shift in scale that degrades accuracy for causal visual-geometry models

Generalized Iterative Closest Point for Pose Refinement **Summer 2024**
NVIDIA Robotics Software Intern *Santa Clara, CA*

- Designed a pose refinement algorithm using generalized iterative closest point method on depth-based truncated signed distance function
- Integrated into the NvBlox 3D reconstruction pipeline

Engineering Projects

RISC-V SoC with Machine Learning Accelerator **September 2020 – December 2020**
Tapeout Class Project *Berkeley, California*

- Used Chipyard to design and tape out a 4-core RISC-V SoC with a sparse machine learning accelerator in Intel 16nm technology
- Generated a digitally controlled oscillator (DCO) using the Berkeley Analog Generator (BAG) and integrated it as an on-chip phase-locked loop (PLL)
- Implemented on-chip reset and clock distribution networks

16-bit Microprocessor with Dot Product Accelerator **September 2020 – December 2020**
VLSI Class Project *Ann Arbor, Michigan*

- Designed and manually laid out a 16-bit RISC-V microprocessor in TSMC 28nm technology

- Implemented and integrated CONV-SRAM, an analog in-memory dot product accelerator for efficient convolution operations

RISC-V R10000 Superscalar Microprocessor **January 2020 – April 2020**

Computer Architecture Class Project *Ann Arbor, Michigan*

- Designed a 2-way superscalar, simultaneous multi-threaded (SMT), out-of-order RISC-V microprocessor based on the R10000 architecture
- Implemented key components including the reservation station (RS), instruction fetch (IF) stage with prefetcher and local branch predictor, and a 2-way set-associative, write-allocate, writeback, non-blocking data cache (D-Cache)
- Developed a cycle-accurate simulator for automated testing and verification

Teaching Experience

EECS251A – Digital Circuit Design **Fall 2022, Fall 2025**

Electrical Engineering and Computer Science *Berkeley, California*

Honors and Awards

2025 NVIDIA Intern Project Showcase Winner

2019 James B. Angell Scholar

Additional Information

- **Computer Skills:** Proficient in C, C++, Python, SystemVerilog, MATLAB, Git, Bash, Virtuoso, and Cadence
- **Languages:** Mandarin Chinese (Native), German (B1 level)